

Figure 1

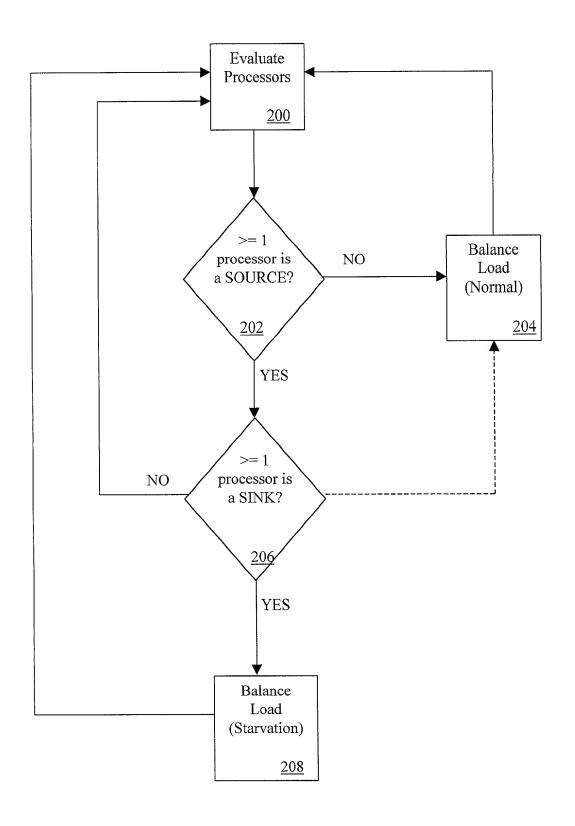
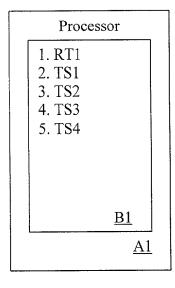
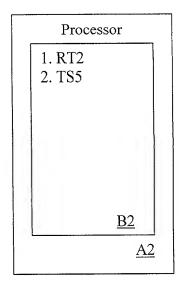


Fig. 2





Processor

1. TS6
2. TS7
3. TS8
4. TS9
5. TS10

B3

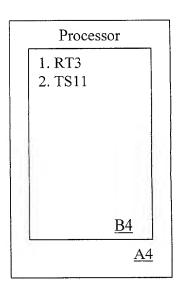
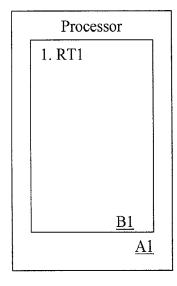
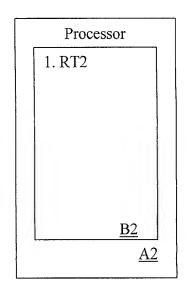


Figure 3





Processor

1. TS6
2. TS7
3. TS8
4. TS9
5. TS10
6. TS1
7. TS2
8. TS3
9. TS4
10. TS5
11. TS11

A3

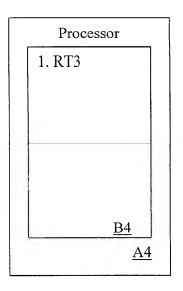


Figure 4

Figure 5